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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,502	11/11/2005	Werner Ertle	1431.124.101/	1444

25281 7590 01/14/2011

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EXAMINER	
HUBER, ROBERT T	
ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
01/14/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,502	ERTLE ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,19,22-39 and 41-44* is/are pending in the application.

4a) Of the above claim(s) *34-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,19,22-33,38,39 and 41-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 26, 2010 has been entered.

Claim Rejections - 35 USC § 112

2. The Examiner acknowledges the amendment(s) to claim 44 filed on October 26, 2010. The rejection of claim(s) 44 under USC 112, first and second paragraph, cited in the previous office action filed on July 26, 2010 is (are) hereby withdrawn.

3. Applicant's arguments, see page 9, filed October 26, 2010, with respect to claim 43 have been fully considered and are persuasive. The rejection of claim 43 under 35 USC 112, first paragraph, has been withdrawn.

Claim Objections

4. Claim 27 is objected to because of the following informalities: The claim recites, as last amended, "*the width (bp) of the test areas*", "*the width of the contact areas*", and "*the length (lp) of the test areas*", all which lack proper antecedent basis. Claim 18, from which claim 27 depends, recites "*width dimensions*" and "*length dimensions*" of the

contact areas and test areas, respectfully, but does not recite "*a width (bp) of the test areas*", "*a width of the contact areas*", and "*a length (lp) of the test areas*". Therefore, "*the width (bp) of the test areas*", "*the width of the contact areas*", and "*the length (lp) of the test areas*" is interpreted as "*a width (bp) of the test areas*", "*a width of the contact areas*", and "*a length (lp) of the test areas*", respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 18, 26 – 28, 39 and 41 - 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strauss (US 5,719,449, prior art of record) in view of Takemae et al. (US 4,744,061, prior art of record).

a. Regarding claim 18, **Strauss discloses a semiconductor chip** (e.g. figures 2 and 3) **comprising:**

a passive first region on a top side of the semiconductor chip (e.g. left side of figure, as clarified in figure below), **the top side of the semiconductor chip defining a plane** (e.g. plain of top side of chip, as seen in figure 3);

an active second region on the top side of the semiconductor chip (e.g. right side of figure 2, as clarified in figure below, with active transistor device comprising elements 204, 205, and 226, col. 2, lines 45 - 48);

an arrangement of contact areas (e.g. contact areas 222. Regarding the term "contact area", this may be regarded as a statement of intended use and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. Indeed, areas 222 may be used as "contact areas") **and test areas** (e.g. test areas 224. Regarding the term "test area", this may be regarded as a statement of intended use and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not

differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. Indeed, areas 224 may be used as "test areas") **having respective top surfaces which are arranged in a common plane that is parallel to the plane of the top side of the semiconductor chip** (e.g. as seen in figure 2, the top surfaces of the contact and test areas are in a common plane (top of line 217), and are parallel to top surface of semiconductor chip), **wherein the top sides of the contact areas are square and have width and height dimensions** (e.g. as seen in figures 2 and 3), **and the top sides of the test areas are rectangular** (e.g. as seen in figure 3, the top sides of the test areas are square, which is a particular shape of a rectangle);

the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane (as seen in figure 2, contact areas 222 and test areas 224 are electrically connect to each other via conduction web 217, col. 2, line 54, which has a top surface in the common plane of the contact and test areas), **the contact areas being arranged in the passive first region** (as clarified in figure below, contact area 222 is in the first passive region), **the passive first region having no active components of an integrated circuit** (as seen in figure below, there are no active components in the first passive region), **the test areas being arranged in the active second region** (as clarified in figure below, the test areas 224 are in the active second region), **the**

active second region having active components of an integrated circuit (as seen in figure below, the active second region has active components of a transistor integrated circuit), **the contact areas are not sealed** (e.g. as seen in figure 2, the contact areas 222 are not sealed);

an insulating layer situated between the top side and a lower plane (e.g. insulating layer 215/216, col. 2, lines 55 – 56, is between the top side and a lower plane);

through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to the lower plane (through contacts 218 are directly below the conduction web 217 and extend from the conduction web to the lower plane), **the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit** (as described in col. 2, lines 45 – 55, where the connection to the components of the integrated circuit are not shown in the figure, are but are disclosed in col. 2, lines 45 - 48);

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts (as seen in figure 2, the portions of insulating layer 215 directly below the contact areas 222 and test areas 224 are free from the through contacts 218).

Strauss is silent with respect to explicitly disclosing the top sides of the test areas have larger length dimensions than the width dimensions of the contact areas. However, Strauss discloses in figure 3 that the areas

corresponding to the interpreted "test areas" (areas 301—305) **appear to have a larger length dimension than the interpreted "contact areas"** (306 - 310).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas have larger length dimensions than the width dimensions of the contact areas since Strauss suggests such a relationship within the figures, and the drawings may be relied up to what they would reasonably teach to one of ordinary skill in the art. See MPEP 2125. Furthermore, it has been held by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47 (CCPA 1976). One would have been motivated to have the test areas larger than the contact areas in order to accommodate different size test probes.

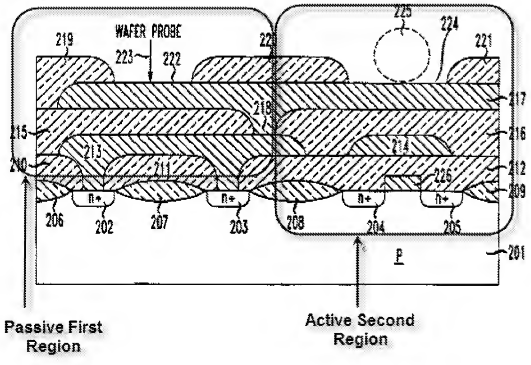
Strauss is also silent with respect to disclosing the test areas are sealed.

Takemae discloses that test areas of electronic devices may be sealed (col. 6, lines 10 - 13).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas are sealed since Takemae discloses that test areas in electronic devices may be

sealed after completion of the device. One would have been motivated to seal the test areas to prevent short circuiting and contamination of the device.

FIG. 2



b. Regarding claim 26, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, as cited above, comprising wherein the conduction web is formed in T** (Strauss: e.g. as seen in figures 2 and 4, a T is formed from the conduction web 217/411 at the interface of the test areas and contact areas) **having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to the width of the contact areas** (Strauss: e.g. as seen in figure 2, the transverse bar of the T 217 has a vertical

width of equal to the vertical width of the contact area 222) **and having through contacts to interconnects** (Strauss: through contacts 55 to interconnects 213), **while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (Strauss: the claim limitation of "*a width determined in response to the maximum current loading*" is considered a process limitation, and the patentability of a product does not depend on the method of production. See MPEP 2113. The width of the longitudinal bar of the T exists and the conduction web is capable of supplying current during testing, therefore the structure anticipates the claimed limitation).

c. Regarding claim 27, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, comprising wherein a width (b_p) of the test areas is about equal to a width of the contact areas and a length (l_p) of the test areas is greater than the width (b_p) of the test areas** (Strauss: e.g. as seen in figure 2, the vertical width of the test areas and contact areas are about equal, and the horizontal length of the test areas is greater than the their vertical width).

d. Regarding claim 28, **Strauss discloses an electronic device** (e.g. figures 2 and 3) **comprising:**

a semiconductor chip having a top side that defines a plane (e.g. plain of top side of chip, as seen in figure 3), **the semiconductor chip having**

an arrangement of contact areas (e.g. contact areas 222. Regarding the term "contact area", this may be regarded as a statement of intended use and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. Indeed, areas 222 may be used as "contact areas") **and test areas** (e.g. test areas 224. Regarding the term "test area", this may be regarded as a statement of intended use and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. Indeed, areas 224 may be used as "test areas") **which are arranged in a common plane that is parallel to the plane of the top side of the semiconductor chip** (e.g. as seen in figure 2, the top surfaces of the contact and test areas are in a common plane (top of line 217), **and are parallel to top surface of semiconductor chip) and are in each case electrically conductively connected to one another via a conduction web that lies in the common plane** (as seen in figure 2, contact areas 222 and test areas 224 are electrically connect to each other via conduction web 217, col. 2, line 54, which has a top surface in the common plane of the contact and test areas), **the contact areas being arranged in a passive, first region of a top side of the semiconductor**

chip (as clarified in figure above, contact area 222 is in the first passive region), **the passive first region having no active components of an integrated circuit** (as seen in figure above, there are no active components in the first passive region), **wherein the contact areas are not sealed** (e.g. as seen in figure 2, the contact areas 222 are not sealed);

the test areas being arranged in an active, second region of the top side of the semiconductor chip (as clarified in figure below, the test areas 224 are in the active second region), **the active second region having active components of an integrated circuit** (as seen in figure below, the active second region has active components of a transistor integrated circuit);

the test areas and contact areas being formed in the same interconnect plane (as seen in figure 2, the test areas 224 and contact areas 222 are formed in the same interconnect plane of the top of the layer 217);

the contact areas being square (e.g. as seen in figures 3 and 4) **with a width approximately equal to the width (bp) of the test areas** (as seen in figure 2, the vertical width of the contact areas 222 are equal to the vertical width of the test areas 224 since they are made from the same layer 217);

an insulating layer situated between the top side and a lower plane (e.g. insulating layer 215/216, col. 2, lines 55 – 56, is between the top side and a lower plane);

through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web

to the lower plane (through contacts 218 are directly below the conduction web 217 and extend from the conduction web to the lower plane), **the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit** (as described in col. 2, lines 45 – 55, where the connection to the components of the integrated circuit are not shown in the figure, are but are disclosed in col. 2, lines 45 - 48);

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts (as seen in figure 2, the portions of insulating layer 215 directly below the contact areas 222 and test areas 224 are free from the through contacts 218).

Strauss is silent with respect to disclosing the test areas having a length (lp) being at least approximately 1.5 times greater than a width (bp) thereof. However, as seen in figure 2, the horizontal length of the test areas is at least greater than the vertical width.

Although the figure is not indicated to be drawn to scale, it would have been obvious for one of ordinary skill in the art at the time the invention was made to make the structure of Strauss such a that the horizontal length of the test areas are at least approximately 1.5 times greater than their vertical width, since often the thickness (vertical width) of the layers are much thinner than the (horizontal) length of the layers, and the figures imply such a configuration for the device. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves

only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make such a modification in order to accommodate a large test probe while having a thin layer in order to minimize device thickness.

Strauss is also silent with respect to disclosing the test areas are sealed.

Takemae discloses that test areas of electronic devices may be sealed (col. 6, lines 10 - 13).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas are sealed since Takemae discloses that test areas in electronic devices may be sealed after completion of the device. One would have been motivated to seal the test areas to prevent short circuiting and contamination of the device.

e. Regarding claim 39, **Strauss discloses a semiconductor chip** (e.g. figures 2 and 3) **comprising:**

a passive first region on a top side of the semiconductor chip (e.g. left side of figure, as clarified in figure above with respect to claim 18), th**e top side of the semiconductor chip defining a plane** (e.g. plain of top side of chip, as seen in figure 3);

an active second region on the top side of the semiconductor chip (e.g. right side of figure 2, as clarified in figure above, with active transistor device comprising elements 204, 205, and 226, col. 2, lines 45 - 48);

an arrangement of contact areas (e.g. contact areas 222. Regarding the term "contact area", this may be regarded as a statement of intended use and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. Indeed, areas 222 may be used as "contact areas") **and test areas** (e.g. test areas 224. Regarding the term "test area", this may be regarded as a statement of intended use and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. Indeed, areas 224 may be used as "test areas") **which are arranged in a common plane that is parallel to the plane of the top side of the semiconductor chip** (e.g. as seen in figure 2, the top surfaces of the contact and test areas are in a common plane (top of line 217), and are parallel to top surface of semiconductor chip) **and are in each case electrically conductively connected to one another via a conduction web that lies in the common plane** (as seen in figure 2, contact areas 222 and test areas 224 are electrically connect to each other via conduction web 217, col. 2, line 54, which has a top surface in the common plane of the contact and test areas), **the contact areas being arranged in the passive first region** (as clarified in figure above, contact

area 222 is in the first passive region), **the passive first region having no active components of an integrated circuit** (as seen in figure above, there are no active components in the first passive region), **the test areas being arranged in the active second region** (as clarified in figure above, the test areas 224 are in the active second region), **the active second region having active components of an integrated circuit** (as seen in figure above, the active second region has active components of a transistor integrated circuit), **wherein the contact areas are not sealed** (e.g. as seen in figure 2, the contact areas 222 are not sealed), **and wherein the top sides of the contact areas are square and have width and height dimensions** (e.g. as seen in figures 2 and 3) **and the top sides of the test areas are rectangular** (e.g. as seen in figure 3, the top sides of the test areas are square, which is a particular shape of a rectangle);

and an insulating layer situated between the top side and a lower plane (e.g. insulating layer 215, col. 2, lines 55 – 56, is between the top side and a lower plane);

through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to the lower plane (through contacts 218 are directly below the conduction web 217 and extend from the conduction web to the lower plane), **the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit** (as described in col. 2,

lines 45 – 55, where the connection to the components of the integrated circuit are not shown in the figure, are but are disclosed in col. 2, lines 45 - 48);

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts (as seen in figure 2, the portions of insulating layer 215 directly below the contact areas 222 and test areas 224 are free from the through contacts 218).

Strauss is silent with respect to explicitly disclosing the top sides of the test areas have larger length dimensions than the width dimensions of the contact areas. However, Strauss discloses in figure 3 that the areas corresponding to the interpreted "test areas" (areas 301—305) **appear to have a larger length dimension than the interpreted "contact areas"** (306 - 310).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas have larger length dimensions than the width dimensions of the contact areas since Strauss suggests such a relationship within the figures, and the drawings may be relied up to what they would reasonably teach to one of ordinary skill in the art. See MPEP 2125. Furthermore, it has been held by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47 (CCPA 1976). One would have been motivated to

have the test areas larger than the contact areas in order to accommodate different size test probes.

Strauss is also silent with respect to disclosing the test areas are sealed.

Takemae discloses that test areas of electronic devices may be sealed (col. 6, lines 10 - 13).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas are sealed since Takemae discloses that test areas in electronic devices may be sealed after completion of the device. One would have been motivated to seal the test areas to prevent short circuiting and contamination of the device.

f. Regarding claim 41, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, as cited above, wherein each of the contact areas is electrically conductively connected to a respective one of the test areas by the conduction web extending between and in the same plane as the contact area and the respective test area** (Strauss: e.g. conducting web 217, which has a top surfaces that is in the common plane as the test areas 224 and contact areas 222).

g. Regarding claim 42, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, as cited above, further comprising a**

boundary defining the area of the semiconductor chip (e.g. as seen in figure 3 of Strauss, the semiconductor chip has an outer boundary); **a continuous metalized area situated within the boundary** (e.g. as seen in figure 2 of Strauss, metalized area comprising layer 217); **wherein the contact areas and the test areas are formed on the metalized area** (contact and test areas 222 and 224 formed on the metalized area of 217, as seen in figure 2 of Strauss), **wherein the contact areas and the test areas are situated within the boundary of the semiconductor chip** (Strauss: e.g. as disclosed in col. 3, line 15 and lines 23 – 26).

h. Regarding claims 43 and 44, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, as recited above. However, Strauss does not explicitly state the test areas are sealed with a patterned photoresist layer (claim 43) or a soldering resist layer (claim 44). However, Takemae discloses the test areas to be sealed after completion of the device** (col. 6, lines 10 - 13).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss in view of Takemae such that the layers that seal the test area are made of a patterned photoresist layer or soldering resist layer since Kim discloses the layers surrounding the test areas to be insulating layers (e.g. layers 53 and 57, disclosed in col. 3, liens 33 and 44), and it is well-known in the art that photoresist and soldering resist are made of

insulating materials, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use photoresist or soldering resist since these materials are well-known insulating materials, and aid in the manufacturing of the device (photoresist) or help localize the solder of contacts that may be formed on the areas (soldering resist).

8. Claims 19, 22 – 25 and 29 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strauss in view of Takemae as applied to claim 18 above, and further in view of Henson (US 6,133,054, prior art of record).

a. Regarding claim 19, **Strauss in view of Takemae disclose the device of claim 18, as cited above, respectively, wherein the insulating layer** (Strauss: figure 2, layer 215/216) **is arranged between the components of an integrated circuit** (Strauss: components 204, 205, and 226) **and the test areas of the semiconductor chip** (Strauss: test areas 224). **Strauss in view of Takemae is silent with respect to disclosing the insulating layer includes silicon dioxide and/or silicon nitride.**

Henson discloses that insulating layers in semiconductor devices may including silicon dioxide or silicon nitride (col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss in view of Takemae such that the insulating layers including silicon dioxide and/or silicon nitride since

Strauss discloses the layers to be insulating, and it was well-known in the art that insulating layers used in semiconductor devices may be formed from silicon oxide or silicon nitride, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide and/or silicon nitride as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

b. Regarding claim 22, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, as cited above, but is silent with respect to the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy.**

Henson discloses that interconnects to electrodes of components of an integrated circuit may comprise copper (e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use copper for the material of the interconnect structure of Strauss in view of Takemae since it was well-known in the art that copper can be used for interconnects in test circuits for integrated circuits, as

disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use copper as an interconnect structure since is a low-resistance conductor that is relatively inexpensive.

c. Regarding claim 23, **Strauss in view of Takemae disclose the semiconductor chip of claim 18, as cited above, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a insulation and passivation layer** (Strauss: layer 219/220/221, disclosed col. 2, lines 57 – 58). **Strauss in view of Takemae is silent with respect to disclosing the insulating and passivation layer is a multilayer structure.**

Henson discloses that insulation and passivation layers on semiconductor devices may be formed as a multilayer structure (e.g. figure 7, layers 722 and 724, disclosed in col. 4, lines 30 - 32).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the structure of Strauss in view of Takemae such that the top insulation and passivation layer comprises multiple layers since Henson discloses a similar device with multiple insulating and passivation layers form atop the device. One would have been motivated to form a multilayer

insulation and passivation layer in order to form a multilayer protection layer that is resistant to physical stress, moisture (as discussed in Henson, col. 4, line 30), and is thermally stable.

d. Regarding claim 24, **Strauss in view of Takemae and Henson disclose the semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer includes a layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web** (e.g. layer 219/220/221 of Strauss, or layers 722 and 724 of Henson).

Strauss, Takemae and Henson are silent with respect to the layer being silicon dioxide. However, Henson discloses that insulating layers within a semiconductor device may include silicon dioxide (col. 4, line 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss in view of Takemae and Henson such that the insulating layer on the top of the device includes silicon dioxide since Henson discloses that silicon dioxide may be used as insulating layers within semiconductor devices, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide as an insulating layer

since it is a common and easily manufactured insulation material, with well-known properties.

e. Regarding claim 25, **Strauss in view of Takemae and Henson disclose the semiconductor chip of claim 23, as cited above, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer** (Henson: col. 4, lines 22 - 23 and lines 31 - 32).

f. Regarding claim 29, **Strauss in view of Takemae disclose the device of claim 28, as cited above, respectively, wherein the insulating layer** (Strauss: figure 2, layer 215/216) **is arrange between the components of an integrated circuit** (Strauss: components 204, 205, and 226) **and the test areas of the semiconductor chip** (Strauss: test areas 224). **Strauss is silent with respect to disclosing the insulating layer includes silicon dioxide and/or silicon nitride.**

Henson discloses that insulating layers in semiconductor devices may including silicon dioxide or silicon nitride (col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss in view of Takemae such that the insulating layers including silicon dioxide and/or silicon nitride since Kim simply discloses the layers to be insulating, and it was well-known in the art that insulating layers used in semiconductor devices may be formed from silicon

oxide or silicon nitride, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide and/or silicon nitride as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

g. Regarding claim 30, **Strauss in view of Takemae and Henson disclose the electronic device of claim 29, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy** (Henson: e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 – 23).

h. Regarding claim 31, **Strauss in view of Takemae and Henson disclose the electronic device of claim 30, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer** (e.g. Strauss: layer 219/220/221, disclosed col. 2, lines 57 – 58 is at the edges of the test areas and contact areas, and on the top side of the conduction web. Figure 7 of Henson shows a

multilayer insulation and passivation layer, including layers 722 and 724, disclosed in col. 4, lines 30 – 32.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the structure of Strauss in view of Takemae such that the top insulation and passivation layer comprises multiple layers since Henson discloses a similar device with multiple insulating and passivation layers form atop the device. One would have been motivated to form a multilayer insulation and passivation layer in order to form a multilayer protection layer that is resistant to physical stress, moisture (as discussed in Henson, col. 4, line 30), and is thermally stable).

Strauss, Takemae, and Henson are silent with respect to the multilayer insulation and passivation layer including silicon dioxide. However, Henson discloses that insulating layers within a semiconductor device may include silicon dioxide (col. 4, line 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss in view of Takemae and Henson such that the insulating layer on the top of the device includes silicon dioxide since Henson discloses that silicon dioxide may be used as insulating layers within semiconductor devices, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945).

One would have been motivated to use silicon dioxide as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

i. Regarding claim 32, **Strauss in view of Takemae and Henson disclose the electronic device of claim 30, as cited above, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer** (Henson: col. 4, lines 22 - 23 and lines 31 – 32).

j. Regarding claim 33, **Strauss in view of Takemae and Henson disclose the semiconductor chip of claim 29, as cited above, comprising wherein the conduction web is formed in T** (Strauss: e.g. as seen in figure 4, a T is formed from the conduction web at the interface of the test areas and contact areas) **having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to a width of the contact areas** (Strauss: e.g. as seen in figure 2, the transverse bar of the T has a vertical width of equal to the vertical width of the contact areas since they are mad from the same layer 217) **and having through contacts to interconnects** (Strauss: through contacts 218 to interconnects 213), **while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (the claim limitation of "*a width determined in response to the maximum current loading*" is considered a process limitation, and the patentability of a

product does not depend on the method of production. See MPEP 2113. The width of the longitudinal bar of the T exists and the conduction web is capable of supplying current during testing, therefore the structure of Kim in view of Henson anticipates the claimed limitation).

9. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Strauss (US 5,719,449, prior art of record) in view of Kim et al. (US 6,159,826, prior art of record) and in view of Takemae et al. (US 4,744,061, prior art of record). **Strauss discloses a semiconductor wafer** (e.g. figures 2 and 3) **comprising:**

a semiconductor chip (chip as seen in figures 2 and 3) **having a top side that defines a plane** (e.g. top side of chip as seen in figures 2 and 3) **and a passive first region** (left side of figure, as clarified in the figure above with respect to claim 18) **and an active second region** (right side of figure, as clarified in the figure above), **the semiconductor chip having an arrangement of contact areas** (contact areas 222. See intended use statement in claim 18 regarding interpretation of contact areas) **and test areas** (test areas 224. See intended use statement in claim 18 regarding interpretation of test areas) **which are arranged in a common plane that is parallel to the plane of the top side of the semiconductor chip** (e.g. top surface of the test and contacts areas are in a common plane that is parallel to the top of the chip) **and are electrically conductively connected to one another via a conduction web that lies in the common plane** (e.g. conducting web of layer 217 under layer 220, which has a top surfaces that is in the common plane as the test areas and contact areas 222 and

224), **wherein the contact areas are not sealed** (as seen in figure 2, the contact area 222 may be considered to be not sealed since it's top surface is exposed);

the contact areas being arranged in the passive first region of the top side of the semiconductor chip (contact areas 222 are in the passive region), **the passive first region having no active components of an integrated circuit** (as seen in figure above, there are no active devices in this region), **wherein the top sides of the contact areas are square and have width and height dimensions** (e.g. as seen in figures 2 and 3); **and**

the test areas being arranged in the active second region of the top side of the semiconductor chip (test areas 224 are in the active region), **the active second region having active components of an integrated circuit** (e.g. as seen in figure above, the active second region has a transistor comprising source 204, drain 205, and gate 226), **wherein the top sides of the test areas are rectangular** (e.g. as seen in figure 3, the top sides of the test areas are square, which is a particular shape of a rectangle); **and**

an insulating layer (insulating layer 216) **having through contacts** (through contact 218) **arranged in the region of the conduction web and extending from the conduction web to a lower plane** (as seen in figure 2), **the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit** (e.g. vias connected to interconnects 213 and the components of the integrated circuit as described in col. 2, lines 45 - 48);

wherein the contact areas and the test areas are free from the through contacts (as seen in figure 2, the contact and test areas are free from the through contacts);

the semiconductor chip being defined by a boundary around the respective semiconductor chip (e.g. outer boundary as seen in figure 3)**, the contact areas and the test areas are completely situated within the boundary of the respective semiconductor chip** (as seen in figure 3, and disclosed in col. 3, line 15 and lines 23 - 26, the test areas and contact areas are within the boundary of the semiconductor chip).

Strauss is silent with respect to explicitly disclosing the top sides of the test areas have larger length dimensions than the width dimensions of the contact areas. However, Strauss discloses in figure 3 that the areas corresponding to the interpreted "test areas" (areas 301—305) **appear to have a larger length dimension than the interpreted "contact areas"** (306 - 310).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas have larger length dimensions than the width dimensions of the contact areas since Strauss suggests such a relationship within the figures, and the drawings may be relied up to what they would reasonably teach to one of ordinary skill in the art. See MPEP 2125. Furthermore, it has been held by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47 (CCPA 1976). One would

have been motivated to have the test areas larger than the contact areas in order to accommodate different size test probes.

Strauss is silent with respect to disclosing the semiconductor wafer comprises a plurality of semiconductor chips.

Kim discloses that semiconductor chips may be formed in plurality on a wafer (e.g. as seen in figures 3 and 4).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the there was a plurality of semiconductor chips since it was well-known in the art that a plurality of semiconductor chips are formed on a single wafer, and then separated into individual chips, as disclosed by Kim. One would have been motivated to form a plurality of chips on a single wafer to increase the efficiency of manufacturing by manufacturing several devices simultaneously on a single wafer.

Strauss is also silent with respect to disclosing the test areas are sealed. However, Strauss discloses the test areas are partially sealed (e.g. the test areas may be considered to be partially sealed since the bottom is sealed by layer 216, and the tops are partially sealed by layer 220/221).

Takemae discloses that test areas of electronic devices may be sealed (col. 6, lines 10 - 13).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the test areas are sealed since Takemae discloses that test areas in electronic devices may be sealed after

completion of the device. One would have been motivated to seal the test areas to prevent short circuiting and contamination of the device.

Response to Arguments

10. Applicant's arguments with respect to claims 18, 28, and 39 have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's arguments filed October 26, 2010 did no properly address the rejection with respect to claim 38. In particular, claim 38 was previously rejected as being obvious over Strauss in view of Kim and Takemae (e.g. see pages 14 - 17 of the office action filed July 26, 2010). However, the Applicant's arguments were primarily addressed to the rejection of claim 18, whereby the Examiner rejected the claim as being obvious over Kim in view of Strauss and Takemae. In particular, the Applicant argues the interpretation of elements of Kim as primary teachings for claim 18. However, as cited above, the rejection of claim 38 uses Strauss as a primary reference to teach most of the elements of the claim. Since the Applicant has not addressed the rejection of the claims with respect to the Strauss reference, there are no arguments presented with respect to the Strauss reference that need the Examiners response. Furthermore, as cited above, the Examiner finds, upon amendment, that Strauss in view of Kim and Takemae still render obvious the claimed invention of claim 38. In particular, the Examiner broadly interprets the amendment citing the "length dimensions" and "width dimensions" of the test areas and contact areas to be a "horizontal length" and

"vertical width", as cited above with respect to claim 38. The Examiner finds that Strauss discloses the horizontal length of the test areas to be larger than the vertical width of the contact areas, and therefore renders obvious the newly amended limitation of the test areas having a larger length dimension than the width dimension of the contact areas. Furthermore, Strauss shows in both figures 3 and 4 that the top sides of the contact areas and test areas are square, and hence further renders obvious the new limitation of the test areas are rectangular (square) and the contact areas are square.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Friday (11am - 7pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 2892
January 5, 2011